d) removing the second barrier layer formed at the bottom of the feature; and

e) selectively depositing a metal layer on the underlayer exposed in the feature.

16. (Twice Amended) The method of claim 15, wherein the first barrier layer and the second barrier layer comprise Si_xN_y.

17. The method of claim 16, wherein the first barrier layer and the second barrier layer are formed using chemical vapor deposition techniques.

18. The method of claim 17, wherein the second barrier layer is removed from the bottom of the feature by sputter etching techniques.

21. The method of claim 15, wherein the metal layer comprises copper.

23. The method of claim 15, wherein the metal layer is deposited using electroplating techniques.

REMARKS

This is intended as a full and complete response to the Office Action dated April 25, 2001, having a shortened statutory period for response set to expire on July 25, 2001. Claims 15-18, 21, and 23 were considered and stand rejected by the Examiner. Applicants assert no new matter has been introduced in this amendment.

Claims 15-18, 21 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi et al.* (U.S. Patent No. 5,308,793) in view of *Zhao et al.* (U.S. Patent No. 5,674,787) and *Sliwa et al.* (U.S. Patent No. 4,962,060). The Examiner states that it would have been obvious to form a titanium nitride layer on the underlying interconnect of *Taguchi et al.* for the disclosed intended purpose of *Zhao et al.* of serving as an anti-reflective coating and/or as an electromigration/stress migration suppression layer, and to selectively deposit the

copper layer on the titanium nitride layer in order to form a copper interconnect. Applicants respectfully traverse this rejection.

Taguchi et al. discloses deposition of a first barrier layer on the sidewalls of a hole in order to reduce oxidation of a second barrier layer of titanium and provide an improved wetting surface for aluminum fill of a hole. *Taguchi et al.* teaches conformal deposition of the second barrier layer on the bottom and sidewalls of the feature and requires the formation of two barrier layers on the sidewalls of a hole.

Zhao et al. discloses forming a dielectric encapsulation layer on the sidewalls of a feature and depositing a seed layer on an underlying metal for electroless fill of a via. *Sliwa et al.* discloses the use of sidewall spacers of a conductive material on an aluminum interconnect to improve oxide planarization and inhibit whisker formation and voiding due to electromigration in aluminum interconnect formation.

Taguchi et al., *Zhao et al.*, and *Sliwa et al.*, alone or in combination, do not teach, show, or suggest depositing a first barrier layer over a blanket dielectric layer, forming a feature through the first barrier layer and the dielectric layer to expose an underlayer, depositing a second barrier layer on the bottom and sidewalls of the feature, removing the second barrier layer formed at the bottom of the feature, and selectively depositing a metal layer on the underlayer exposed in the feature. Therefore, the references, alone or in combination do not teach, show, or suggest claimed aspects of the invention. Withdrawal of the rejection is respectfully requested.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest claimed aspects of the invention. Having addressed all issues set out in the office action, applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

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APPENDIX

15. (Fourth Amendment) A method of filling a feature in a dielectric layer, comprising:

a) depositing a first barrier layer over a blanket dielectric layer;

b) forming a feature through the first barrier layer and the dielectric layer to expose an underlayer;

c) depositing a second barrier layer on a bottom and sidewalls in the feature;

d) removing the second barrier layer formed at the bottom of the feature; and

e) selectively depositing a metal layer on the underlayer exposed in the feature.

16. (Twice Amended) The method of claim 15, wherein the first barrier layer and the second barrier layer [are comprised of] comprise Si_xN_y.